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(54) System and multiplexer/ demultiplexer for the transmission/ reception of digital television information.

(57) It is described a system and related multiplexers/demultiplexers for the transmission/reception of digital television information (video + audio), included the high definition information (HDTV), in which it is used the transmission in packets and various work speeds are foreseen, among which a special transmission that uses two data flows transmitted contemporaneously for getting a sole information. The multiplexer is associated to external buffers that receive the data at different speeds, form the packet and generate requests of transmission to the multiplexer that receives them according to preestablished priorities.

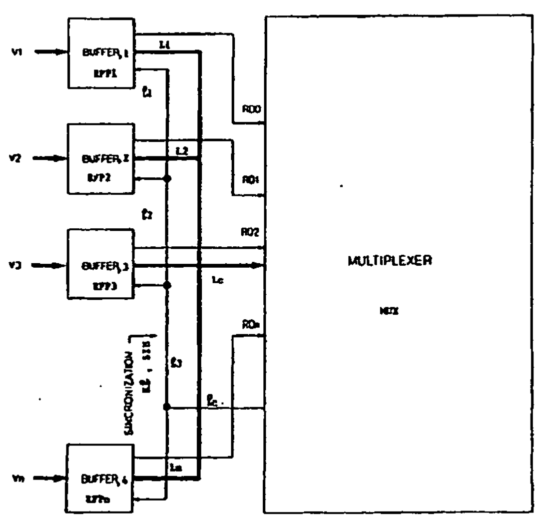

Fig1

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SYSTEM AND MULTIPLEXER/DEMULTIPLEXER FOR THE TRANSMISSION/RECEPTION OF DIGITAL TELEVISION INFORMATION

DESCRIPTION OF THE INVENTION

The present invention refers to a system for the transmission/reception of digital television information (video + audio), in particular for the high definition television information (HDTV). The invention includes also the multiplexers/demultiplexers used for the embodiment of said system.

The multiplexing/demultiplexing systems usually order the data in transmission at a fixed distance in the frame and separate the data in reception according to this preestablished sequence. Yet, in the case the data must be transmitted at different speeds, the operations become more complex and the classic system cannot be used. Until to-day it is not available a system suitable for solving this problem, caused by the necessity of transmitting data series with different speeds.

The first aim of the present invention is to provide a simple and efficient system for transmitting data with different speeds. A further scope of the invention is to provide a multiplexer/demultiplexer structure that is particularly suitable for the related system.

The system according to the invention is now characterized in that the data at different speeds are no more transmitted unchanged directly to the multiplexing stage, but they are collected externally to the multiplexer in packet forming means of preestablished structure; each time said means have formed a packet they send a request to the multiplexing stage; the different sources are supplied with different priorities, therefore, in the case of contemporaneous transmission requests, it is satisfied the request coming from the packet source that is associated to higher priority.

The Figures 1 and 2 show the transmission, respectively reception schemes of the system according to the invention. The data at different speeds V1, V2, ...Vn arrive separately to the packet collectors-formers RFP1, RFP2....RFPn, in this case formed by buffer stores 1, 2, 3.... n, that are joined by means of the lines L1...Ln and the line in common with the multiplexer MUX. According to the invention, when one of the buffers (e.g. 1) reveals that a data number suitable to be transmitted exists, that is a number equal to the packet-length, the request RQo to the MUX is generated for informing MUX that the packet is available and for having the consent for the transmission thereof. The MUX processes the request coming from RQo together with the possible other contemporaneous request coming from RQ1 to RQn and, if these have not higher priorities than the priority assigned to RQo, it allows the output of the data packet accumulated with speed V1 into the buffer 1. The higher priority shall correspond in our case to the data concerning the audio, followed by the fixed data of the video part. After these data are transmitted, the codes having a variable length coming from processors and as last data, the data having the lowest speed and importance as the telex transmissions, the ancillary data, etc. are transmitted. These priorities can be changed in any moment. Each time it is recognized the transmission request RQi, MUX ge nerates the corresponding timings and synchronisms K1, and SIN:MUX communicates with the circuits forming the packets by means of the lines l_1, l_2, li.

The data transmission is carried out after having made a redundancy insertion for a future error correction by means of a FEC (Forward Error Corrector).

In reception (Figure 2) the circuit must recognize the buffer 1', 2'... n' to which each received packet is destined.

For making this, it is used the definition of the packet type hold in the initial part of the same packet (as it shall be indicated in the Figure 9, that allows to understand how the frame and packets must be formed) assigning well-established packet types to each area. For allowing the changing and programming of this information according to the future requirements of the total system, the output decision is not taken by the demultiplexer DEMUX in a fixed manner, but it provides said information, after having extracted it from the frame, to an external circuit deciding the destination of the same information PAL, using the bus PT. TAL decides in relation to the assignment table supplied case-by-case (that can be changed easily as indicated for the priority RQi) and provides the destination signal of the packet by means of the bus OS.

According to the information sent by OS, the demultiplexer DEMUX decides the type of synchronism and timings K'1, SIN' that it must generate for the data output; these signals are transmitted onto the lines l'i, l'1...l'n, while the information is transmitted onto the lines L'1, L'2...L'n.

As data output speeds and according to the quantity of information to be transmitted, the following channel speeds are foreseen:

1 channel with 34 Mbits/s
2 channels with 34 Mbits/s
1 channel with 140 Mbits/s

Each possibility provides the more quality the more the speed is owing to the evident greater

data quantity that can be trasmitted keeping constant the transmission time interval.

Considering the first two cases, all multiplexing/demultiplexing part is processed in the semicustom circuit, and considering the last case, owing to the high speed of the final stages, the series-parallel or parallel-series conversions and the interfaces of the lines are foreseen externally using ECL logics. The information distribution is based on frames (Figure 9) formed by two data packets having 238 words of 16 bits, and further a first head word that holds the above mentioned definition of the packet type in the first 8 bits, said information being protected by a Hamming code, error corrector, and further 16 redundancy words of 16 bits for the error correction.

The frame shall be started with an alignment word of 24 bits, and further 8 bits that shall be formed by a status word provided by an external system.

the continuation of the alignment word shall be formed by an information of 16 bits, that shall be the information allowing to recover the video synchronism in reception. All these data shall be transmitted in the form words of 8 bits even if they can be grouped in words having a greather or shorter length after the buffers.

In the case it is used 34 Mbit/s speed, the running of mux/demux is similar to a normal system, excepting the matter that the data transmission is carried out in packets and not according to a fixed sequence. The demultiplexing is made revealing the alignment word and in the moment of the alignment acquisition the initial heads of the packets are revealed and the information related to the area that must receive the transitted packet is extracted. In the case it is used 140 Mbit/s speed, the data are multiplexed in MUX, but the series and the line code conversions are applied externally to the circuit in the ECL logics for obvious reasons of work speed; in reception the data enter in DEMUX, already transformed by parallel conversion, directly to the input elastic store and they follow the above said normal process.

The more interesting part is that related to 2*34 Mbits/s, in which two independent channels C1, C2 (respectively C'2, C'2) are used for transmitting the whole information. Until to-day, for increasing the data speed to be transmitted by a system, a higher data hierarchy was used with the following necessity of using a transmission means having a higher frequency. This fact requires to use, e.g. in the case of radiocommunications, more and more high channels with consequent problems of the increasing frequency, included in the microwave field.

In our case a speed of 2x34 Mbits/s with 8 bits words is advantageously used, but the following explanation is referred to a generical system.

The system according to the invention allows to use a well established hierarchy for transmitting an information with double speed using two independent flows for the transmission of a sole information. In this manner it can be advantageously used the same type of (doubled) transmission means without the necessity of having an access to order higher means.

According to a feature of the invention, the information is divided in two flows separating a part from the other part and rejoining these parts in reception for obtaining the original information. For acting in this manner, it is necessary to synchronize the two independent flows and compensate the time differences between the flows for the different delays to which they are submitted owing to the differences in the tranmission means.

The Figure 3 represents schematically the system according to the invention. In transmission the word of N bits, Fri, is divided in two word of N/2 bits, F1, F'1. Owing to the dif ferences in the transmission time TO and the delay changes, the two flows F1 and F'1 arrive with delays DELAY1 and DELAY2, in addition to the speed changes.

In reception these changes must be compensated for turning to the original words of N bits.

According to a feature of the invention, as indication of the difference between the transmission times of the two flows, it is used the information obtained from the time difference at the apparition of the alignment word.

In transmission a channel C1 transmits the N/2 bits of greater weight of the word of N bits and the second channel C2 transmits the other N/2 bits of less weight (e.g. see Figure 1). In reception the following factors must be considered:

- each channel shall have different delays for being dependent, therefore the time differences between the two information must be compensated, as above said;
- as further performance it can be added a revelation of the channel fixing each information.

This second possibility foresees the introduction of an alignment word revelation different in each channel, generating a high or low channel indication. In this manner the input channel changes are compensated automatically.

For compensating the delay a more complex process is applied, that can be understood better with reference to the Figures 4, 5 and 6. The Figure 4 shows the input flows F1, F1', that are now introduced into an elastic store Me with different clocks. The name of elastic store means that it is a store where the reading-writing distance is variable, the data being introduced by means of a clock and the data being read by means of a second clock.

The aim of a memory of this type is to absorb

the instantaneous changes of the writing clock and further, in our case, to synchronize the bits, as the writing foresees a clock for each flow, while the reading uses a same master clock in the two memories. Obviously a PLL must be used for getting that the writing and reading frequencies are equal, for avoiding fillings and emptyings of the elastic store ME, that, as above said, must absorb the instantaneous changes. Therefore the output of the elastic store shall provide two synchronized information along the duration of bits, read in the two flows by the same clock, as it is shown in Figure 4. Therefore it shall be obtained a synchronization at clock level and a new alignment at bit level. Each of information (packets PA11...PA21; respectively PA12..PA22) is transmitted to an alignment detector that provides the words correctly aligned and formed as they were originally, owing to the detecting of the alignment word, and so it can be known the right bit for each word being started. Therefore at the input of the alignment generator RI, as it is shown in Figure 5, two flows can be got (represented by the continuous line) that must be aligned correctly.

The words shall be aligned correctly at output, but it exists a time difference between the apparition of the alignment words in each flow. This difference supplies the mean value of the delay between the two frames that shall be compensated. Until this moment it was got the word synchronism.

For understanding as the time difference is compensated, it must be defined a flow as master flow and the other flow as slave flow. The master flow is the flow that was joined to the circuit clock frequency. The difference between the apparition of the alignment works in the secondary flow can be positive or negative with respect to the master flow, that is it can be in advance or delay. In other words the time difference can be positive or negative. It is revealed the time difference between the apparition of two alignment words. This difference must be compensated. For making this, the master flow is always delayed of a fixed value T, so that the alignment word appears always at output shifted by T words after the detecting thereof.

The slave flow can be moved in advance or in delay with respect to the other flow. For discovering this, the alignment detector starts a counter for each of the flows. At the moment in which the alignment word appears in the two channels, the time difference between the two channels shall be given by the difference between two counters CNT1-CNT2 (CNT1 - counter of the master channel, CNT2 - counter of the slave channel). This value can be positive or negative, according to the circumstance that the alignment word appeared in master channel or in slave channel for the first time.

This value is named D, so that:
CNT1-CNT2 = D

As above said, the master flow was delayed of a fixed value T, therefore it is obtained that, at the instant t01, the alignment word appears in the master channel and in the instant t02 the same word appears in the slave channel. The difference between the two times shall be:

t01 - t02 = D*tp ; [1]

where tp is the duration of a word.

The alignment word after the delay shall appear at the time t0t1, given by the expression:

t0t1 = t01 + T*tp ;

The slave channel shall include a delay TS that provides the output at the instant t0t2, given by:

t0t2 = t02 + TS*tp ;

The solution that it looked for is that t0t1 = t0t2, from which:

t0t1 = t01 + T*tp]
] t01 + T*tp = t02 * TS*tp ;
t0t2 = t02*TS*tp]
TS*tp = t01 - t02 + T*tp ;
replacing [1]:
TS*tp = D*tp + T*tp ;
TS = D + T

Therefore it shall be foreseen a variable delay line, in which it is assumed that the minimum value of TS = 0, (to delay the signal of a negative number shall be equivalent to accelerate it), therefore:

D + T = 0 ;
- T < D < T
from which:
0 < TS < 2T;

In our case, the value of T was selected equal to 64 therefore, as words are treated, it shall be present a delay of 64*4 bit = 256 bit; TS being variable between 0 and 512 bit, that in the case of 2*34 Mbit/s shall provide a time of bit equal to 1/34 µs and a delay compensation of 256*1/34,368 µs = 7.5 µs in advance or delay.

Comparing this value of total frame time, that should have a length (always for our particular application):

2*(238*16 + 16 + 16 + 16) + 2*16 + 16 = 8208 bits

with a frame time for 2*34 Mbits/s equal to:

8208*1/(2*34.368) Is. = 119.413 µs

Expressing the compensation in other manner, it can be seen as:

256/8208 = 3.118 %

The embodiment of the variable delay line allows two variants:

- a memory in which the reading-writing distance fixes the delay thereof;
- a shift register line, forming the delays of 2 ^ N and selecting the delay to be applied by means of a multiplexer selection. As preferred fulfilment form it was used the second option, whose implementa-

tion is easier .A representation of the embodiment forms of the two options is visible in Figures 7 and 8 respectively.

At the output of the delay lines it shall be obtained the frame synchronism, by which, always considering that the delay difference between the two frames is lower than the fixed value, it shall be obtained tht the two channels are completely synchronized. In the case in which it is not possible to compensate the delay, it is generated an external alarm.

This alarm must reveal only tht the absolute value of D is higher than the maximum foreseen value.

As it can be noticed in the Figure 6, at output of the system SC of delay compensation, it is got that the two frames are completely synchronized and the sole action that must be done is to join the two words of N/2 bits in words of N bits for reconstructing the original information.

Another performance that is foreseen by the circuit is the possibility of working as a "repeater" introducing directly the data from another demultiplexer and using an external selection to replace the packets that are required in the point of the distribution network and inserting further the supplementary information in the packets that in transmission were let free just for realizing this possibility, as above indicated.

This is got by means of the data introduction by another bus and, in the case of revelation of a "replaceable" packet, it is replaced with one of the packets fixed externally.

For resuming and fixing better the ideas:

- Figure 3 shows the flow fu formed by words having a N length, that at the time TO is divided in two flows F1 and F1′ having words of N/2 length. F1 arrives to the demulitplexer DEMUX at the moment TO + delay 1, F′1 arrives AT TO + delay 2; DEMUX joins again F1 and F′2 compensating the respective delays 1 and 2 and forming again the original flow F′n of words having a N length;
- Figure 4 represents the elastic store ME that carries out the new alignment at bit level between F1 and F2 and the synchronization at clock level;
- Figure 5 represents the tester RI of synchronzation and therefore at word level;
- Figure 6 shows the compensation system with new alignment at packet level;
- Figure 7 represents the variable delay line (for compensating the delay of Figure 6) made with classic system, that is a store that receives the data in input IN and sends them at output OUT with a delay that is equal to the distance between reading and writing; for this aim the writing is controlled by the counter WC, whose counting, added with the delay TS, controls the reading;
- Figure 8 shows the delay line that is advantageously formed by a series of MUX preceded by registers that supply shifts 2^N, 2^(N-1)-...respectively 1. The first MUX receives the signal at input IN, the signal from the register with shift 2^N and the signal of a LATCH fed by the delay signal TS. Each of MUXs following the first MUX shall receive the signals from the preceding MUX, from the decreasing shift register 2^(N-1) etc. and from the LATCH;
- Figure 9 shows the formation scheme of two exemplifying packets (first, second packet PAC1, PAC2).

A particularly simple and advantageous embodiment form foresees tht the frame is really formed by two packets PAC1, PAC2 of 255 words formed each of 16 bits; the head of each packet foresees two words of 16 bits reserved to the alignment words (24 bits) ALIN1, ALIN2, ALIN3, and to the status word (STATUS) (8 bits) and further two 16 bit words for the video synchronism (VIDEO FREC). Each packet is protected by an error correction code (FEC). The first 16 bits of each packet hold the information related to the source from which the same packet comes (PACKET TYPE). The transmission from the buffer store Bi to the multiplexer MUX and from the demultiplexer DEMUX to the buffer B′i occurs by means of the 8 bit words (P1, P2). It was noticed before that the multiplexer can run with three different speeds: 1 flow with 34 Mb/s; 2 flows with 34 Mb/s; 1 flow with 140 Mb/s. In the first two cases all of operations of a multiplexer-demultiplexer are advantageously made internally to the semicustom circuit, while in the third case the series/parallel conversion and the interface of lines are carried out externally by ECL logics owing to the very high speed. In the case 2 flows with 34 Mb/s are used, it is got the advantage to work with a frequency double of 34 Mb/s, but using the transmission speed of 34 Mb/s onto two independent flows.

For getting the original information, the two flows are joined in reception in a correct manner, synchronizing the two input flows. The 8 bit words in transmission are divided in two 4 bit words (the most significant 4 sits and the less significant 4 bits), and transmitted independently. In reception it is possible to recognize the most significant bits and the less significant bits (as it is necessary to recognize different alignment words) being possible, in this manner, to compensate eventual channel exchanges. The two received flows are recorded in two elastic stores with different writing clocks extracted from flows and are read with the same clock, that is the one related to the master flow (Figure 4). Then it is present an alignment

generator RI (Figure 5) in each path and at output from each alignment generator a correctly aligned flow is got; as a time difference between the position of the alignment word can be present in a flow with respect to the other flow, it is compensated from the variable delay line SC (Figure 6) that, in the preferred fulfilment form of Figure 8, has registers inserted by means of MUX.

As above indicated, the system can run as repeater, in which case the free packets are replaced with the desired packets.

For aims of illustrative clearness the invention was described with reference to the fulfilment forms represented in drawings; obviously different variants, modifications and replacements and the like can be applied without outgoing from the spirit or scope of the invention.

Claims

1) A transmission system for TV, HDTV, audio and data signals, that come from different sources and can have speeds different with one another and arrive to a centralized part (multiplexer), characterized in that in transmission the signals at different speeds are each accumulated into a proper buffer, that forms the packet therewith and, when the packet is ready, requires to the centralized part (multiplexer) the enabling for transmitting the said packet; the multiplexer fulfils the request according to a prefixed priority order and adds to the packet a frame synchronization signal forming in this manner at least a data flow that can be also transmitted with at least a speed that can be selected in a range suitable for existing carrier waves; and in reception it carries out the new alignment of the information flow(s) onto the basis of the synchronization signal and after the packets are distributed to the various buffers and then to the related receivers.

2) A system according to claim 1, characterized in that the running of the multiplexer is foreseen with three different speeds in particular one flow with 34 Mb/s - two flows with 34 Mb/s, one flow with 140 Mbit/s.

3) A system according to claim 2, characterized in that the information is transmitted in two paths.

4) A system according to claim 1, characterized in that the free packets are replaced with interested packets causing the system to run as repeater.

5) A system substantially according to what described and represented.

6) An apparatus for the fulfilment of the system according to preceding claims, characterized in that it includes:

- means for feeding information flows with different speeds to means forming data packets;
- a multiplexer for multiplexing and transmitting one of said packets one at a time by at least one channel;
- means for assigning the priority to packet forming means;
- means for interrogating the multiplexer and for enabling this last multiplexer to transmit the packet with greather priority.

7) An apparatus according to claim 6, in which the transmitter includes a series of buffers in a number equal to the number of speeds of different channels; one multiplexer; linkages between buffers and multiplexer suitable for generating the priorities; synchronism and clock generators; at least one transmission channel.

8) An apparatus according to claim 7, in which the receiver includes a demultiplexer which is associated to a circuit for packet decision and destination; a series of buffers, a linkage network from these buffers to the demultiplexer suitable for reestablishing the priorities and a system for synchronization and clock regeneration.

9) An apparatus according to claims 7 and 8, in which the information flow is splitted in two transmission channels, each including one elastic store, one realignment generator and one delay trimmer.

10) An apparatus according to claim 9, in which the trimmer is a variable delay line preferably formed by many registers and multiplexers and one latch.

11) A system and apparatus substantially according to what described and represented.

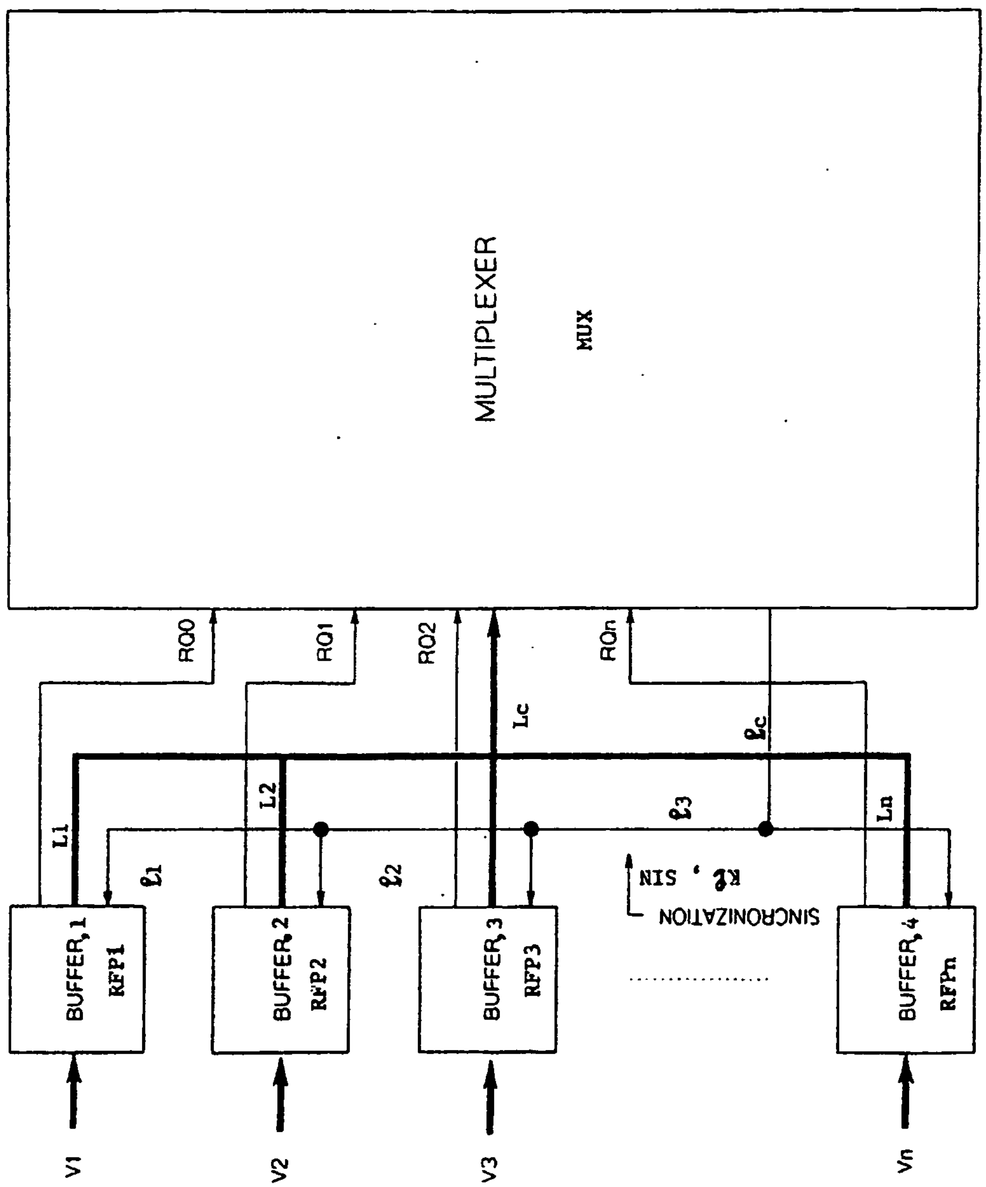
MULTIPLEXER
MUX
RQ0
RQ1
RQ2
RQn
Lc
ℓc
L1
L2
Ln
ℓ1
ℓ2
ℓ3
SINCRONIZATION
Kℓ, SIN
BUFFER 1
RFP1
BUFFER 2
RFP2
BUFFER 3
RFP3
BUFFER 4
RFPn
V1
V2
V3
Vn

Fig.1

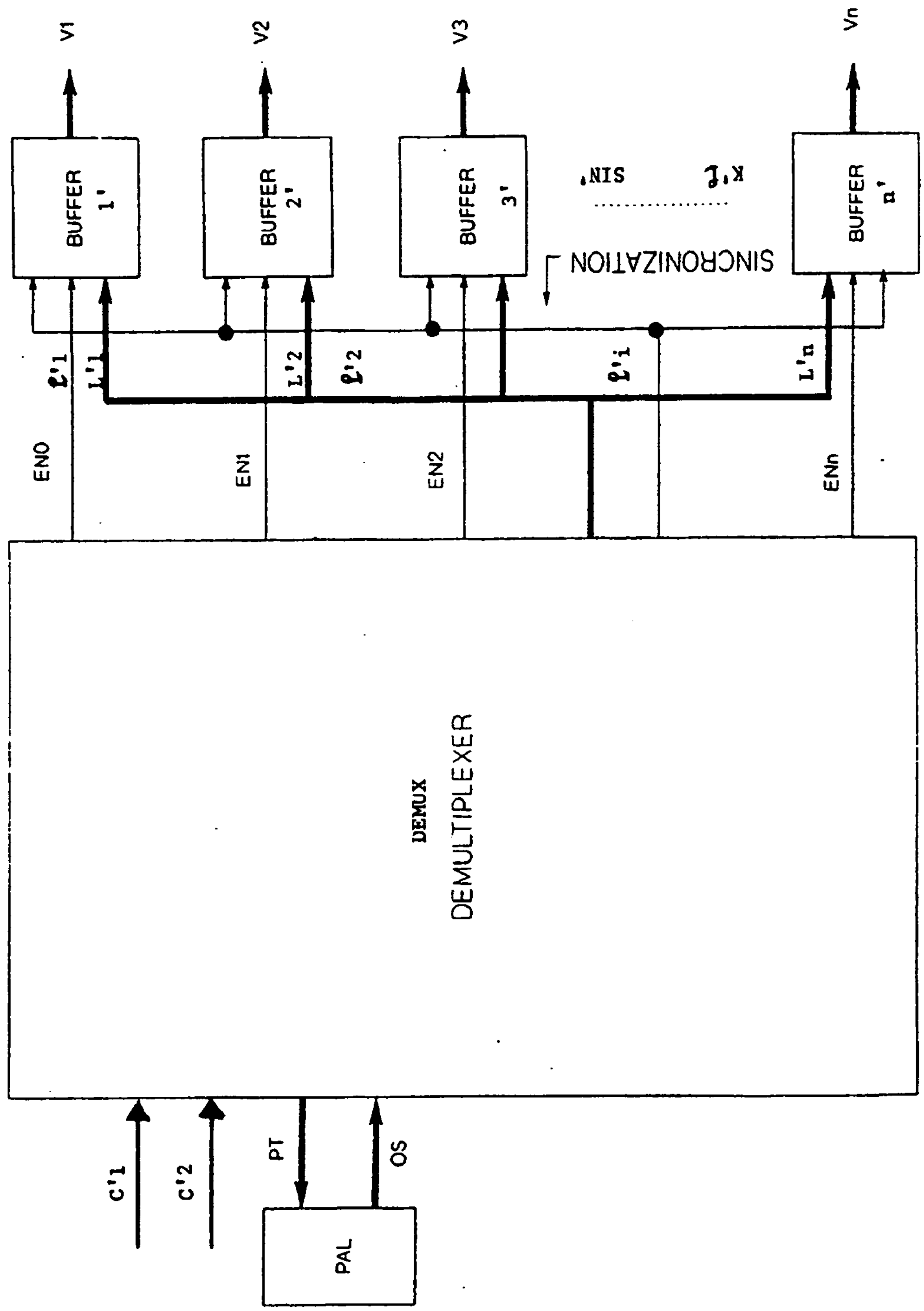
V1
V2
V3
Vn
BUFFER 1'
BUFFER 2'
BUFFER 3'
BUFFER n'
SIN'
K'ℓ
SINCRONIZATION
ℓ'1
L'1
L'2
ℓ'2
ℓ'i
L'n
EN0
EN1
EN2
ENn
DEMUX
DEMULTIPLEXER
C'1
C'2
PT
OS
PAL

Fig. 2

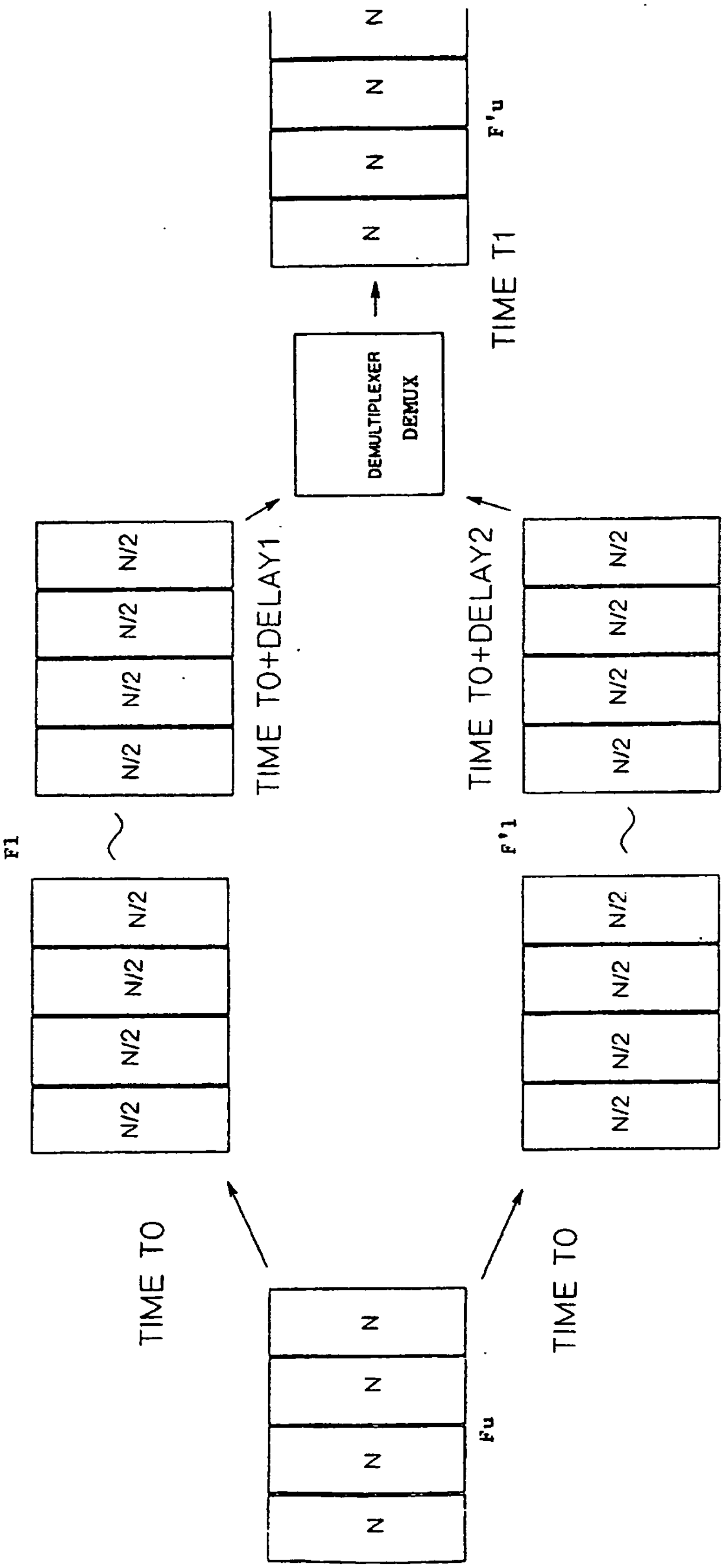
Fu
N
N
N
N
TIME TO
TIME TO
F1
N/2
N/2
N/2
N/2
N/2
N/2
N/2
N/2
TIME TO+DELAY1
F'1
N/2
N/2
N/2
N/2
N/2
N/2
N/2
N/2
TIME TO+DELAY2
DEMULTIPLEXER
DEMUX
TIME T1
F'u
N
N
N
N

Fig. 3

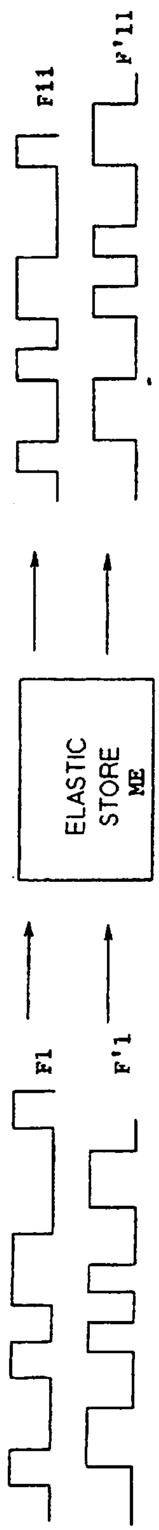

Fig. 4

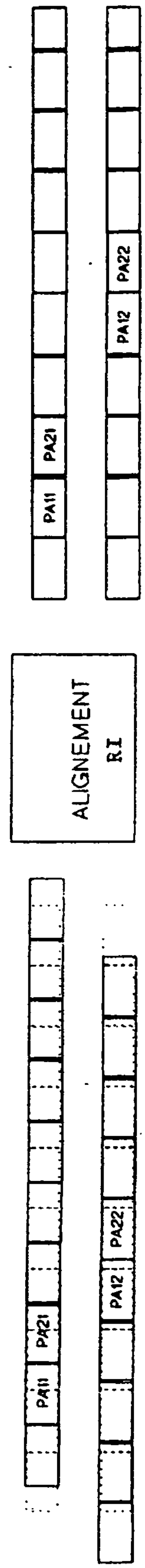

Fig. 5

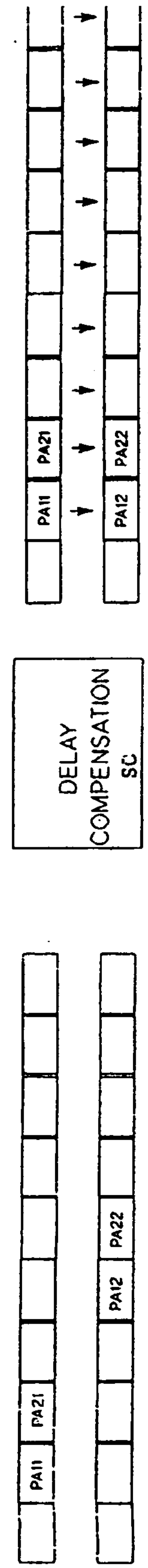

Fig. 6

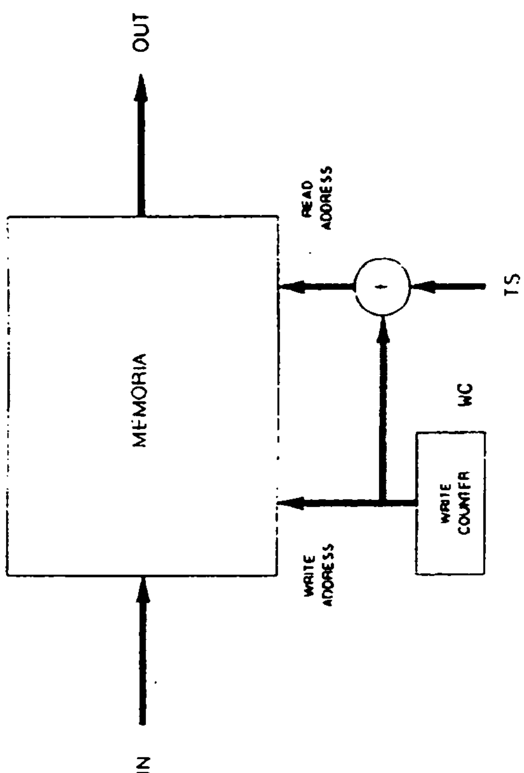
MEMORIA
IN
OUT
READ ADDRESS
WRITE ADDRESS
WRITE COUNTER
WC
TS

Fig. 7

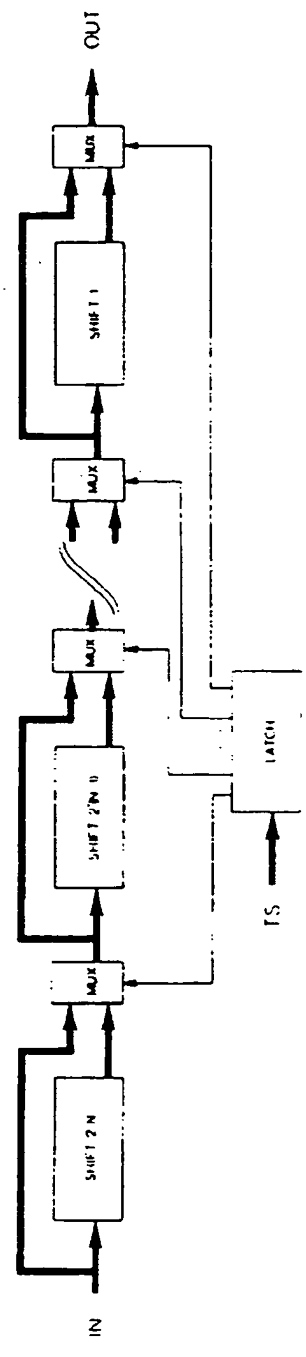
IN
SHIFT 2 N
MUX
MUX
MUX
SHIFT 1
MUX
OUT
LATCH
TS

Fig. 8

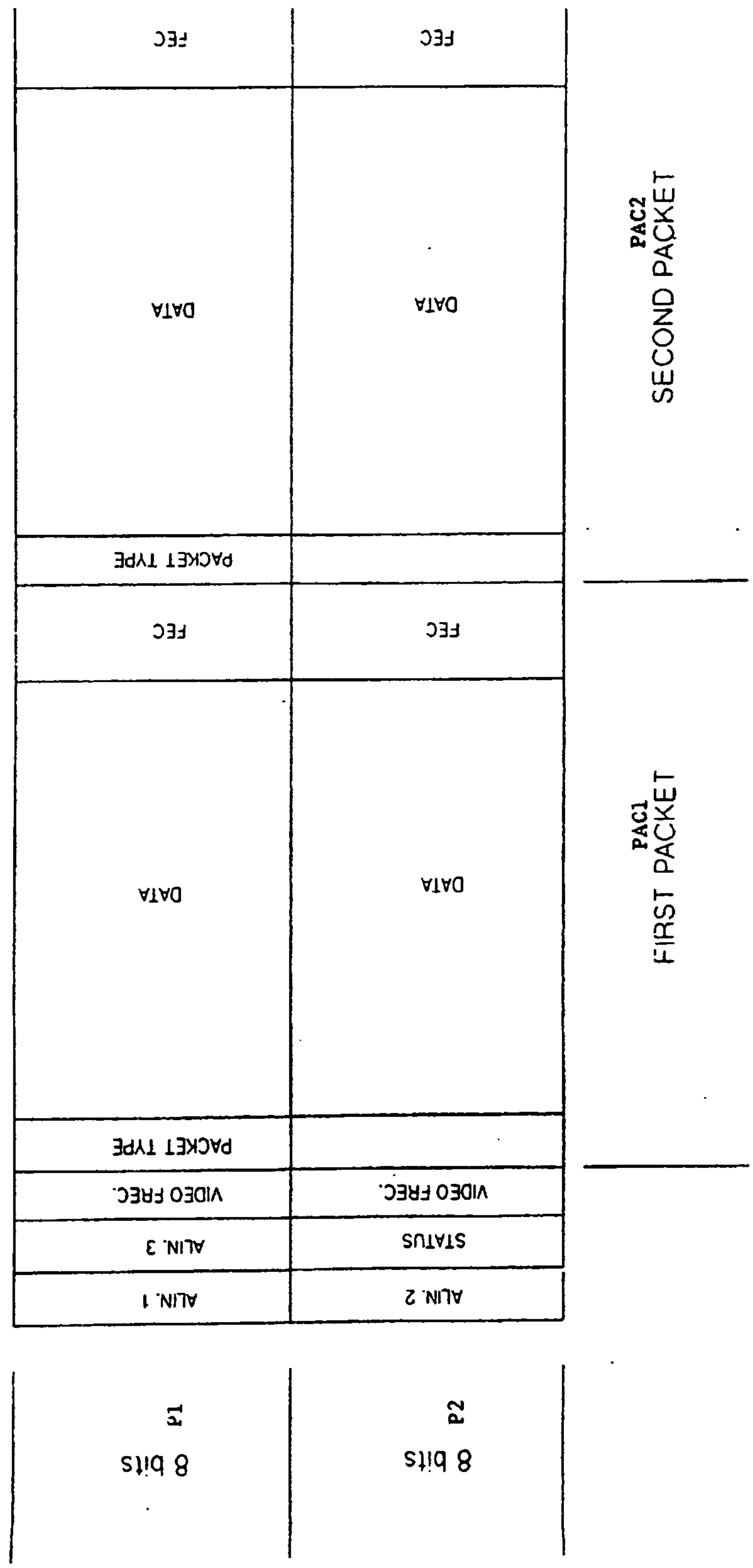
8 bits
P1
8 bits
P2
ALIN. 1
ALIN. 2
ALIN. 3
STATUS
VIDEO FREC.
VIDEO FREC.
PACKET TYPE
DATA
DATA
FEC
FEC
PACKET TYPE
DATA
DATA
FEC
FEC
PAC1
FIRST PACKET
PAC2
SECOND PACKET

Fig. 9